Keysight Technologies
U4154A AXIe-Based Logic Analyzer Module

Data Sheet

KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

Product Description

The Keysight Technologies U4154A AXIe-based logic analyzer system combines reliable data capture with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high-speed digital designs operating at speeds up to 4 Gb/s.

Figure 1A shows the small eyes associated with a DDR3 system operating at 1.4 V at 2133 Mb/s. The U4154A logic analyzer uses its unique eye scan capability to automatically place the sampling point in both time and voltage within the eye on each individual channel for optimal sampling reliability.

Figure 1B shows the trigger setup to capture a burst of 8 data samples. The trigger sequencer operates up to 2.5 Gb/s, enabling accurate and precise triggering.

Figure 1C and Figure 1D show the state listing and waveform for these data captures.

The 12.5 GHz Timing Zoom with 256 K sample memory gives you simultaneous state and high-resolution timing measurements covering a time span of 20 µs, which corresponds to 43680 clock cycles at a 2133 MHz clock rate.

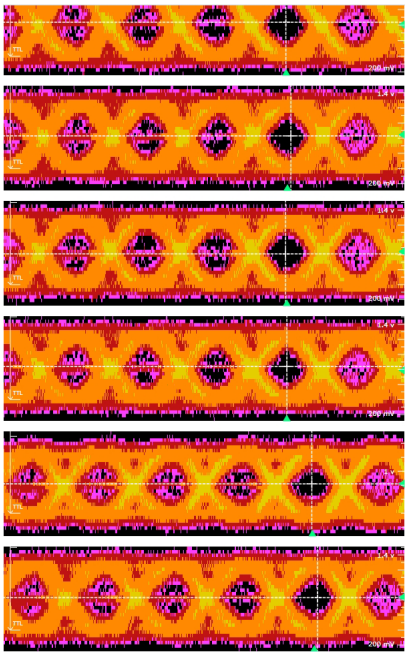


Figure 1A

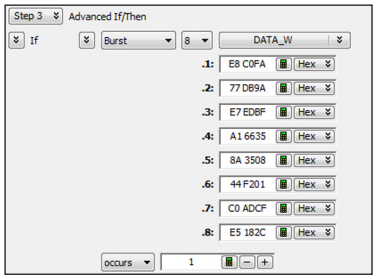


Figure 1B

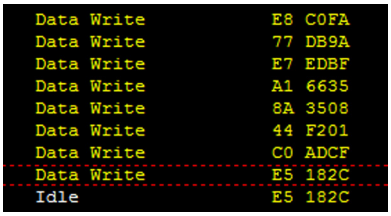


Figure 1C

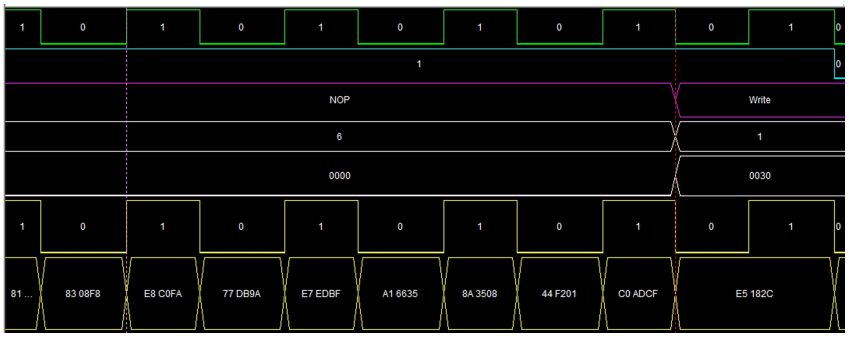


Figure 1D

Product Description (continued)

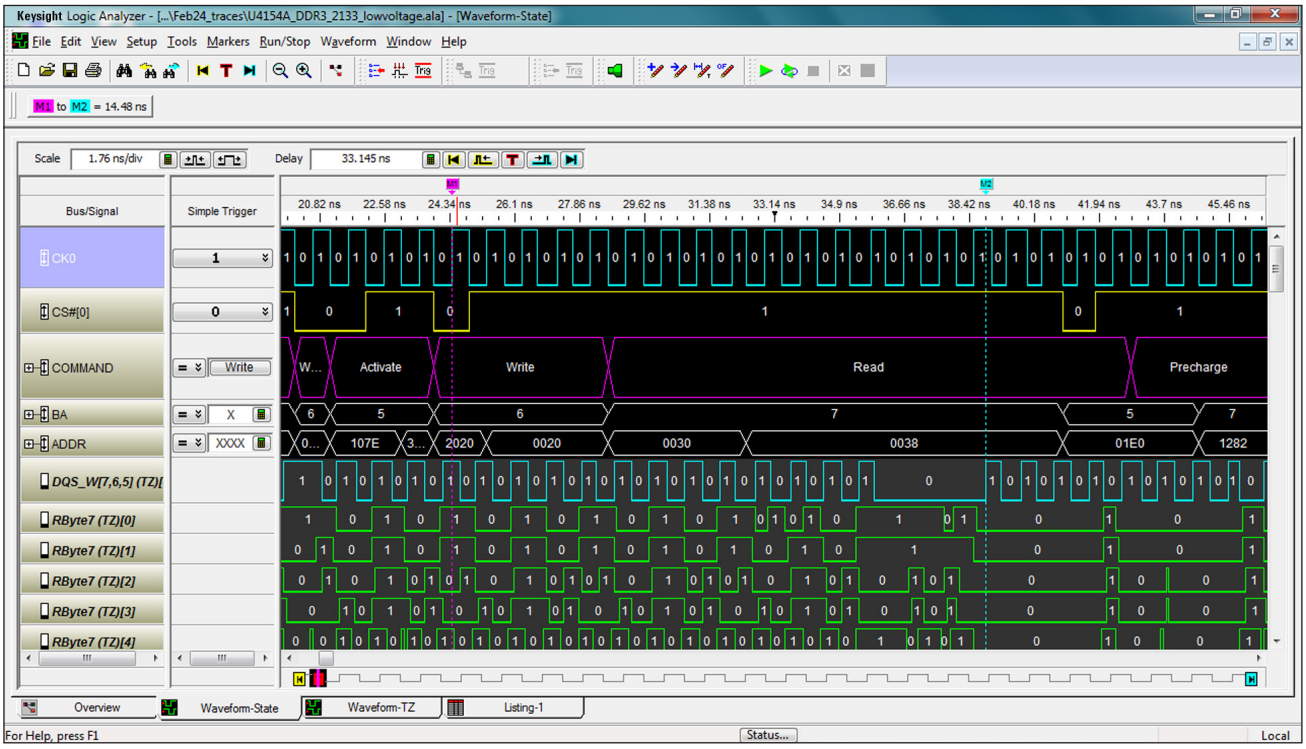


Figure 2. Timing zoom precisely measures the time between the rising edge of the clock and the rising edge of DQS in a DDR system.

Available memory depth up to 200 M samples allows you to debug very complex problems where the cause and symptoms may be separated by several seconds. The amount of memory can upgraded after purchase; see the Upgrades section of the Ordering Information on page 16.

No need to sacrifice sampling resolution to view more system activity. In timing mode, if your system has bursts of activity followed by times with little activity, you can use transitional timing along with the logic analyzer's deep memory to capture seconds to minutes of activity at 400 ps sampling resolution at a sample frequency of 2.5 GHz. You also have the flexibility to increase the amount of time captured by excluding certain buses or signals from the transition detector. For example, you can exclude clock or strobe signals that add little useful information to the measurement. In **State** mode, select **Store Qualification** to save states of interest into memory.

The dual-sample mode for DDR memory signals up to 2.5 Gb/s allows for the separation of reads from writes with automatic setup of the correct sampling positions for each. This mode also allows acquisition of state (synchronous) data at rates up to 4 Gb/s. When used in this mode, the data will appear in two labels. One label for rising edge and another for falling edge captures. The logic analyzer will be clocked with one edge of the system clock. Labels can be merged using the Keysight B4602A Signal Extractor tool. When operated in dual-sample mode on all pods, the channel count is 68 channels for one U4154A, or 136 channels for two U4154As combined. Dual-sample mode can be selected on a per-pod-pair basis, so if you have only a subset of signals that require dual-sample mode, the channel count can be higher.

A burst-mode clock allows you to take measurements that include periods of inactivity on the clock, such as power management transitions when the clock is inactive.

Make faster, easier, more powerful DDR measurements

The DDR setup assistant simplifies measurement setup and minimizes the time to make your first measurement. The DDR setup tool guides you through even the most complex DDR setup in minutes. DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Keysight qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data.

The DDR setup assistant includes a variety of powerful, time-saving trigger features optimized for DDR measurements. Burst trigger captures an entire data burst of 8 data samples on DDR2/3 systems from one sequence level in the trigger menu. Intuitive trigger macros with diagrams provide visualization of triggering options and simplify the process of creating triggers.

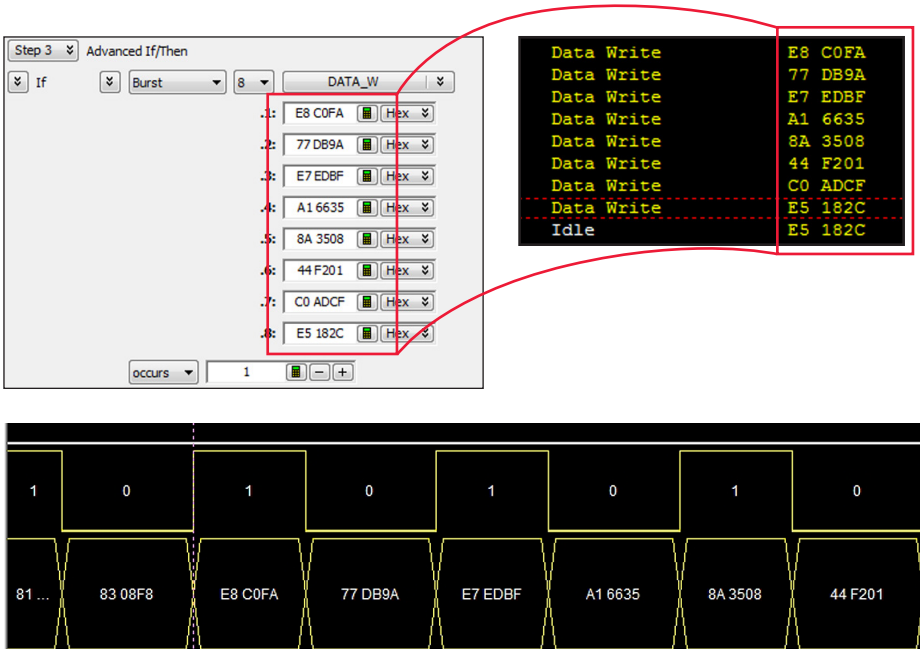


Figure 3. Burst recognizer trigger makes it easy to trigger on events in a burst read or write.

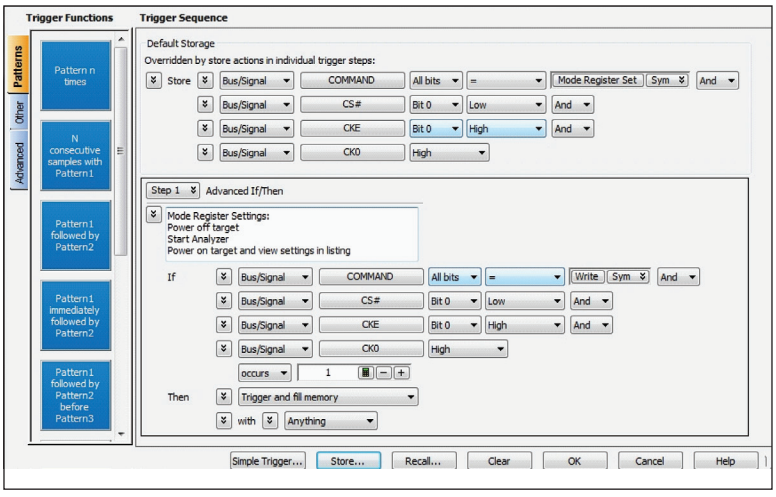


Figure 4. Mode register set trigger allows you to capture key events during initialization without wasting valuable memory.

Improve Signal Integrity with Eye Scan Technology

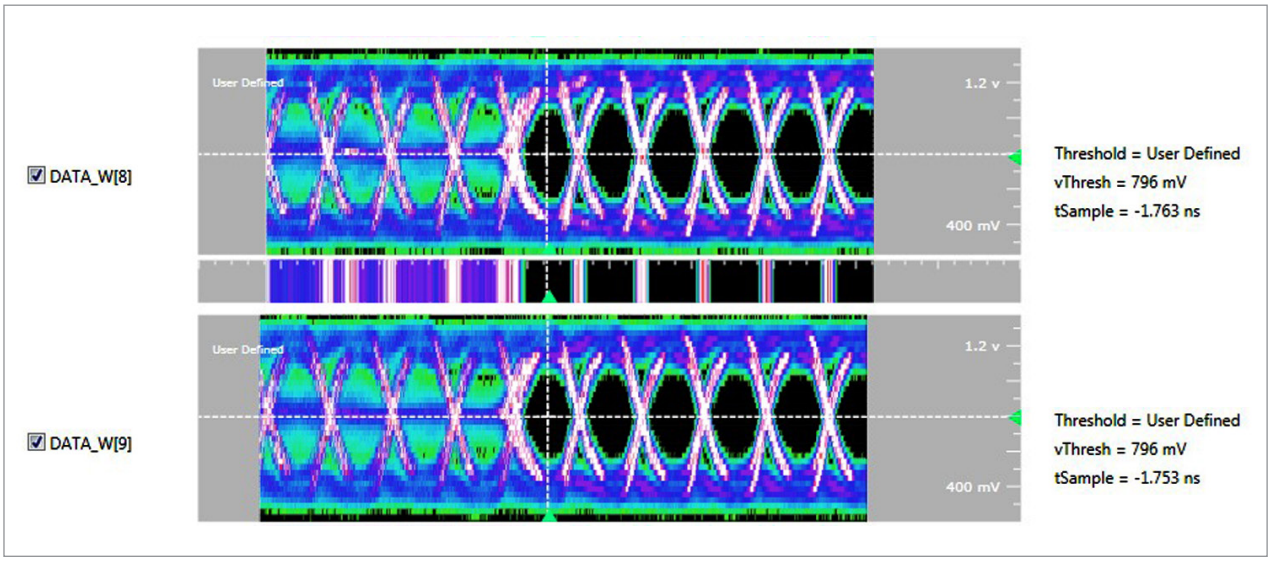


Figure 5. Burst qualified eye scan allows you to view the activity on the signals only when a burst takes place.

As timing and voltage margins continue to shrink, confidence in signal integrity becomes an increasingly vital requirement in the design validation process. Eye scan lets you acquire signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes. Identify problem signals quickly for further investigation with an oscilloscope. Results can be viewed for each individual signal or as a composite of multiple signals or buses. Support up to 4 clock qualifiers, isolate scans of any signal from any combination of other signals, use full-triggering capabilities for scan qualification, and analyze specific system activity with customizable viewing windows to sample only when the qualifying signal is active. The eye scan technology in the U4154A provides insights that can't be achieved with any other test method.

DDR eye scan automatically groups signals so you can quickly spot byte lane-related signal integrity problems. Scans can be qualified based on trigger-state criteria, thus providing unique insight. For example, read and write scans can be separated for greater insight. Burst scan allows you to gather signal integrity information on two read or write cycles separated by only one cycle.

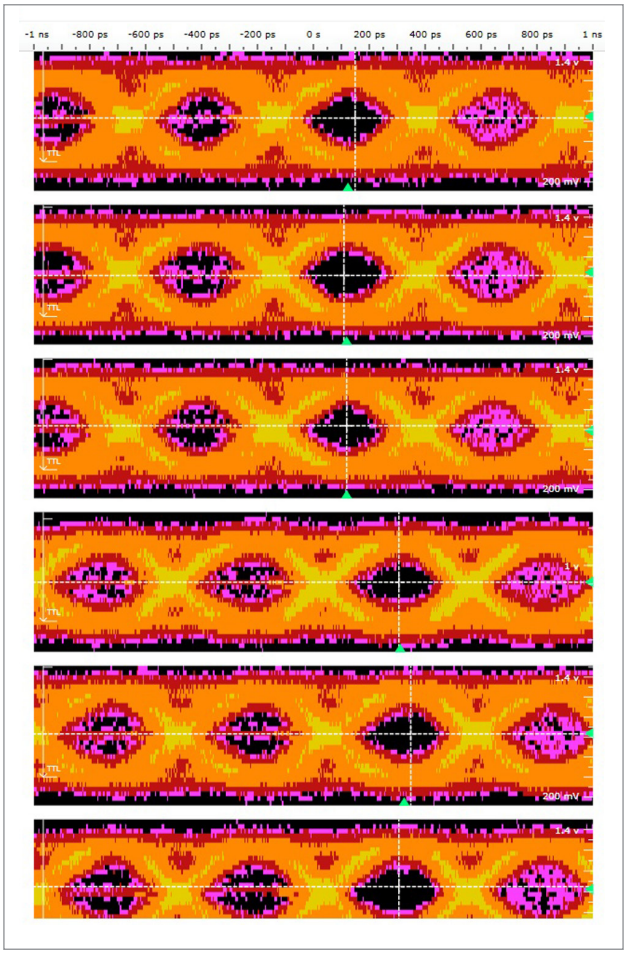


Figure 6. Eye scan clearly indicates the byte lane shift caused by fly-by routing.

Harness your logic analyzer and scope for powerful insight

Combine the powerful triggering and protocol analysis of a logic analyzer with the signal integrity insight of to solve tough design problems. Keysight ViewScope allows you to an oscilloscope easily make time-correlated measurements between Keysight logic analyzers and oscilloscopes. The time-correlated logic analyzer and oscilloscope waveforms are integrated into a single logic analyzer waveform display for easy viewing and analysis. You can also trigger the oscilloscope from the logic analyzer (or vice versa), and automatically de-skew the two instruments.

ViewScope enables you to perform the following tasks more easily, quickly, and effectively:
- Validate signal integrity
- Track down problems caused by signal integrity
- Determine correct operation of A/D and D/A converters
- Access correct logical and timing relationships between the analog and digital portions of a design

Operating modes [1]

Operating mode	Conventional state (synchronous) Option -02G	Conventional state (synchronous) Option -01G (std)	Dual sample state Option -02G	Dual sample state Option -01G (std)	Conventional timing full channel	Conventional timing half channel	Transitional timing full channel	Transitional timing half channel	Timing Zoom
Acquisition rate	2.5 Gb/s	1.4 Gb/s	4 Gb/s	2.8 Gb/s	2.5 GHz	5 GHz	2.5 GHz	5 GHz	12.5 GHz
Number of channels in one U4154A	136	136	68	68	136	68	136	68	136
Number of channels in two U4154As combined	272	272	136	136	272	136	272	136	272
Memory depth (samples) [2]									
Opt 002 (std)	2 M	2 M	2 M	2 M	2 M	4 M	2 M	4 M	256 K
Opt 004	4 M	4 M	4 M	4 M	4 M	8 M	4 M	8 M	256 K
Opt 008	8 M	8 M	8 M	8 M	8 M	16 M	8 M	16 M	256 K
Opt 016	16 M	16 M	16 M	16 M	16 M	32 M	16 M	32 M	256 K
Opt 032	32 M	32 M	32 M	32 M	32 M	64 M	32 M	64 M	256 K
Opt 064	64 M	64 M	64 M	64 M	64 M	128 M	64 M	128 M	256 K
Opt 128	128 M	128 M	128 M	128 M	128 M	256 M	128 M	256 M	256 K
Opt 200	200 M	200 M	200 M	200 M	200 M	400 M	200 M	400 M	256 K

1. Contact Keysight Technologies for information on additional configurations.
2. Memory can be upgraded after purchase. See the Upgrades section of the Ordering Information on page 16.

When you need more channels or more functions

Multiframe allows you to combine 16 plus AXIe chassis.

Note: One PC host is recommended for each AXIe chassis.

Applications

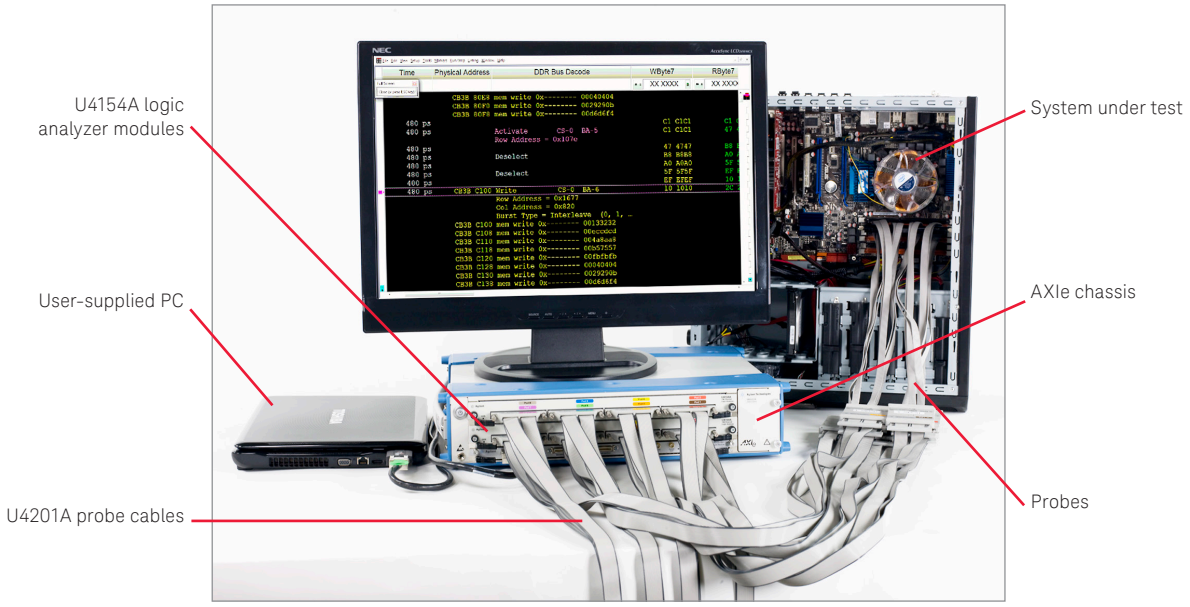
- Functional and parametric validation of memory systems and other high-speed digital systems operating up to 4 Gb/s
- Debug of hardware and software in high-speed digital systems operating up to 4 Gb/s

Features

- State capture up to 4 Gb/s on 68 channels, 2.5 Gb/s on 136 channels per module
- Reliable data capture on eye openings as small as 100 ps by 100 mV
- 12.5 GHz Timing Zoom with 256 K sample memory
- Memory depth up to 200 M samples
- Wide variety of probing solutions including BGA, interposer, mid-bus, and flying leads
- Up to 10,880 channels in a system

Customer values

- Confidence in state measurements with signal eye openings as small as 100 ps by 100 mV
- Rapidly view signal integrity information on all the buses in your design, under a wide variety of operating conditions, in a matter of minutes
- Quickly and easily set up complex DDR measurements



Hardware platform

Minimum hardware

One or more U4154A 136-channel logic analyzer modules. Two U4154As can be combined for a total of 272 channels on a single time base and trigger sequencer. Two U4154As are required to capture all read and write data on a 64 Data bit DDR2/3/4 interface for data rates up to 2.5 Gb/s. DDR2/3/4 solutions requiring 5 pods or less require one U4154A module. LPDDR1/2/3 solutions requiring and operating up to 2.5 Gb/s, 4 pods or less require one U4154A module.

One Keysight M9502A 2-slot or M95905A 5-slot AXIe chassis. Refer to www.keysight.com/find/axie-chassis

One M9536A AXIe Embedded Controller or one user-supplied PC equipped with Microsoft Windows XP (32-bit), Microsoft Windows Vista (32/64-bit), or Microsoft Windows 7 (32/64-bit), and PCIe link or capable of accepting a PCIe adapter.

For laptop PCs
- One Keysight M9045B PCIe ExpressCard Adaptor
- One Keysight Y1200B PCIe cable: x1 to x8, 2.0 m

For desktop PCs
- One M9048A PCIe Desktop Adaptor

Four U4201A logic analyzer probe cables

Probes as required to connect to the target system

Probe type	Model number	Channels	Maximum data rate	Supported signal types
Soft Touch Connectorless Pro Series	E5406A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft Touch Connectorless Low Profile	E5402A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft Touch Connectorless Classic	E5390A	34 (32 data, 2 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft Touch Connectorless Half-Size	E5398A	17 (16 data, 1 clock)	4 Gb/s	Single-ended data, differential or single-ended clock
Soft Touch Connectorless Pro Series	E5405A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock
Soft Touch Connectorless Classic	E5387A	17 (16 data, 1 clock)	4 Gb/s	Differential or single-ended data, differential or single-ended clock
Samtec connector	E5378A	34 (32 data, 2 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock
Samtec connector	E5379A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock
Mictor connector	E5380A	34 (32 data, 2 clock)	600 Mb/s	Single-ended data, differential or single-ended clock
General purpose flying leads	E5382A	17 (16 data, 1 clock)	1.5 Gb/s	Single-ended data, differential or single-ended clock
General purpose flying leads	E5381A	17 (16 data, 1 clock)	1.5 Gb/s	Differential or single-ended data, differential or single-ended clock

Recommended probes for DDR memory include BGA probes, interposers, and Soft Touch mid-bus probes.
Interposers are available from FuturePlus Systems and Nexus Technology.

For more information about FuturePlus probes
www.futureplus.com

For more information about Nexus Technology probes
www.nexustesttechnology.com

For additional DDR/2/3/4 and LPDDR/2/3 probing options, contact your local Keysight representative.
www.keysight.com/find/contactus

Optional Hardware

Multiframe extensions

Additional AXIe chassis, or one or more Keysight 16902B logic analyzer frames with any of the modules that are compatible with the 16900 system. Refer to www.keysight.com/find/16900 and to the 16900 Series Logic Analysis System Mainframes Data Sheet. Up to 16 AXIe or 16902B frames can be combined in a single Multiframe system.

One or more E5861A Multiframe cables to connect multiple frames. Order one fewer E5861A cables than the total number of frames/chassis to be combined.

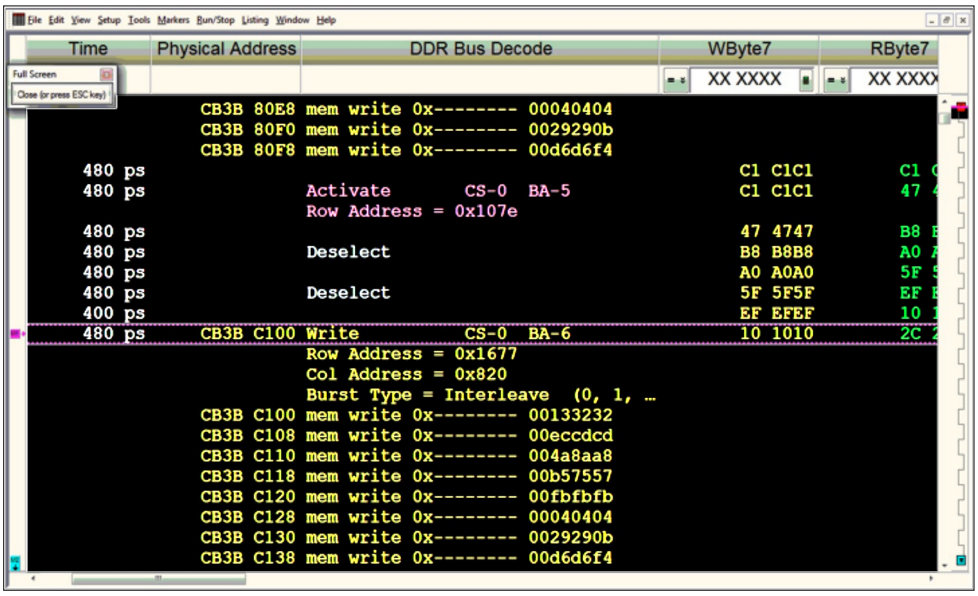


Figure 8. The B4621B protocol-decode software displays acquired signals as easily understood bus transactions.

Optional software

B4622B DDR2/3/4 or LPDDR/2/3 Protocol Compliance and Analysis Tool

Achieve greater protocol insight faster using the B4622B protocol compliance and analysis toolset for DDR2, DDR3, DDR4, LPDDR, LPDDR2, or LPDDR3. The B4622B provides four software tools in one set covering automated real-time violation capture, protocol violations detection on captured traces, performance measurements, and physical address trigger setup for DDR2/3/4 or LPDDR/2/3. Create your own regression test suite for your DDR2/3/4 or LPDDR/2/3 or other digital system monitored by your Keysight logic analyzer. Accelerate your regression test results by adding any valid logic analyzer trigger to customize your suite of automated real-time protocol or bus level timing violations.

Monitor your DDR2/3/4, LPDDR/2/3 or other digital system continuously for elusive, intermittent violations in protocol or bus level timing with your customizable real-time violation capture tool.

Bus decoders for DDR2/3/4 or LPDDR/2/3 validation

The B4621B bus decoder for DDR2, DDR3, visit our web site to find additional analysis software. LPDDR, LPDDR2, or LPDDR3 validation provide complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4621B protocol-decode software translates acquired signals into easily understood bus transactions, with associated data bursts for data rates up to 2.5 Gb/s.

The B4623B bus decoder for LPDDR, LPDDR2, or LPDDR3 validation provides complete protocol decode of memory transactions using a Keysight logic analyzer as the analysis execution engine. The B4623B protocol-decode software translates acquired signals into easily understood bus transactions with associated data bursts, at the full bus speed.

Visit our web site to find additional analysis software.
www.keysight.com/find/logic-sw-apps

Technical Specifications and Characteristics

All specifications refer to the combination of a U4154A Logic Analyzer Module, U4201A logic analyzer probe cable, and any Keysight Soft Touch probe.

State (synchronous) sampling mode	
Maximum state data rate Option U4154A-02G 2.5 GHz state mode (spec)	2.5 Gb/s on 136 channels per U4154A, using either or both edges of clock (spec)
	4 Gb/s on 68 channels per U4154A, clocking on either edge of the clock (typ)
Maximum state data rate Standard U4154A-01G 1.4 GHz state mode (spec)	1.4 Gb/s on 136 channels per U4154A, using either or both edges of clock (spec)
	2.8 Gb/s on 68 channels per U4154A, clocking on either edge of the clock (typ)
Maximum state clock frequency (typ)	
Option U4154A-02G	2.5 GHz
Standard U4154A-01G	1.4 GHz
Minimum state clock frequency[1] (typ)	12.5 MHz (single edge)
	6.25 MHz (both edges)
Sample position adjustment resolution (typ)	
Option U4154A-02G	5 ps or 20 ps
Standard U4154A-01G	20 ps
Sample position adjustment accuracy (typ)	±150 ps
Minimum data valid window (typ)	
Option U4154A-02G	100 ps
Standard U4154A-01G	160 ps
Minimum setup time (typ)	50 ps
Minimum hold time (typ)	50 ps
Minimum eye height (typ)	
Option U4154A-02G	100 mV
Standard U4154A-01G	160 mV
Sample position adjustment range (typ)	7 ns
Minimum state clock pulse width (typ)	200 ps
Number of clocks (nom)	1
Minimum time between active clock edges (typ)	400 ps
Maximum time between active clock edges[1] (typ)	80 ns
Number of clock qualifiers (nom)	4
Clock qualifier setup time (typ)	100 ps
Clock qualifier hold time (typ)	100 ps
Time tag resolution (typ)	80 ps
Maximum time count between stored states (typ)	66 days

1. Clock can pause for up to 66 days once every 8 or more edges.

Technical Specifications and Characteristics (continued)

Timing (asynchronous) sampling mode		
	Half-channel mode	**Full-channel mode**
Maximum sample rate (nom)	5 GHz	2.5 GHz
Minimum sample period (nom)	200 ps	400 ps
Number of channels (nom)		
One U4154A	68	136
Two U4154As combined	136	272
Pod usage (nom) 1 pod from each	1 pod from each odd/even pod pair, user selectable	All pods
Timing Zoom sampling rate (nom)	12.5 GHz	
Timing Zoom memory depth (nom)	256 K samples	
Maximum time between transitions (nom)	66 days	
Minimum data pulse width (typ)	1 sample period + 200 ps	
Time interval accuracy (typ)	± (1 sample period + 400 ps + 0.01% of time interval reading)	
Trigger characteristics		
Maximum trigger sequence speed (typ)		
Option U4154A-02G	2500 MHz (400 ps)	
Standard U4154A-01G	1400 MHz (714 ps)	
Trigger resources (nom)	16 patterns evaluated as =, ! =, >, > =, <, < =	
	8 double-bounded ranges evaluated as in range, not in range	
	4 to 8 burst detectors	
	4 edge detectors in timing, 3 in transitional timing	
	1 occurrence counter persequence level	
	1 timer	
	3 flags	
	1 arm in	
Trigger resource Boolean conditions (nom)	Arbitrary Boolean combinations	
Trigger actions (nom)	Goto	
	Trigger and fill memory	
	Trigger and Goto	
	Trigger, send e-mail, and fill memory	
Store qualification actions (nom)	Default (global) and per sequence level	
	Store/don't store sample	
	Turn on/off default storing	
Timer actions	Start from reset	
	Stop and reset	
	Pause	
	Resume	
Flag actions	Set	
	Clear	
	Pulse set	
	Pulse clear	

Technical Specifications and Characteristics (continued)

Trigger characteristics (continued)	
Maximum trigger sequence levels (nom)	8
Trigger sequence level branching (nom)	Arbitrary 4-way if/then/else
Trigger position (nom)	Start, center, end, or user-defined
Maximum occurrence counter (nom)	999,999,999
Maximum pattern width (nom)	128 bits – single label
	272 bits – AND of multiple labels across two-card set
Maximum range width (nom)	64 bits
Timer range (nom)	100 ns to 27 hours (in timing modes)
	200 * state clock period to 27 hours (in state mode)
Timer resolution (nom)	5 ns
Timer accuracy (typ)	± (5 ns +0.01%) (in timing modes)
	± (8 * state clock period +2 ns +0.01%) (in state mode)
Timer reset latency (nom)	40 ns (in timing modes)
	80 * state clock period (in state mode)
General	
Number of channels (nom)	
One U4154A	136
Two U4154As combined	272
Maximum channels on a single time base and trigger (nom)	272
Number of analyzers (nom)	1
Input signal amplitude V_{amptd} (typ)	≧350 mV
Supported signal types	Single-ended and differential
Voltage threshold (typ)	–5 V to +5 V
Minimum threshold resolution (typ)	
Option U4154A-02G	2 mV
Standard U4154A-01G	20 mV
Threshold accuracy (typ)	± (30 mV + 1% of setting)
Threshold setting granularity	By channel

Technical Specifications and Characteristics (continued)

Environmental and physical

Operating environment	
Temperature (nom)	0 to +40 °C
Humidity (nom)	0 to 80% relative humidity at 40 °C
Altitude	0 to 3000 m
Vibration	Random vibration 5 to 500 Hz, 10 minutes per axis, approximately 0.2 g rms
Non-operating environment	
Temperature (nom)	–40 °C to +75 °C
Humidity (nom)	0 to 90% relative humidity at 65 °C
Altitude	0 to 15,300 m
Vibration (in shipping carton)	Random vibration 5 to 500 Hz
	10 minutes per axis
	Approximately 2.41 grms
	Swept sine resonant search
	5 to 500 Hz
	0.50 g (0 to peak)
	5 minute resonant dwell at 4 resonances per axis
Weight	
Weight	2.34 kg

Definitions for Specifications

Specification (spec): Represents warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 to 40 °C, unless otherwise stated, and after a 45 minute warm-up period. The specifications include measurement uncertainty. Data represented in this document are specifications unless otherwise noted.

Typical (typ): Represents characteristic performance, which 80% of the instruments manufactured will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 25 °C).

Nominal (nom): The expected mean or average performance, or an attribute whose performance is by design, such as the 50 Ω connector. This data is not warranted and is measured at room temperature (approximately 25 °C).

Measured (meas): An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift versus time. This data is not warranted and is measured at room temperature (approximately 25 °C).

Configuration Information

Recommended configuration for DDR2/3 analysis		
Model	**Quantity**	**Description**
U4154A-02G [1]	2 [1]	Logic Analyzer, 136-channel 12.5 GHz timing zoom 2.5 GHz state, 2 Mb depth
M9502A	1	AXIe 2-slot chassis
U4201A	8	Logic analyzer probe cable
M9536A	1	AXIe Embedded Controller or M9045B
M9045B or M9048A	1	PCIe ExpressCard Adaptor for laptops; PCIe Desktop Adaptor
Y1200B or Y1202A	1	PCIe cable: x1 to x8, 2.0 m for use with M9045B; PCIe cable: x8, 2.0 m for use with M9048A [1]
Probes		As required, refer to ordering information

1. Only 1 required for solutions requiring up to 5 pods for DDR2/3/4 pods for LPDDR/2/3.

Up to 3 module sets can be installed in one M9505A 5-slot AXIe chassis. A module set is defined as any of the following:

- One U4154A
- Two U4154As combined into a single time base and trigger
- One U4301A PCIe analyzer
- One U4998A HDMI protocol analyzer/generator (PAG) module

Slot 5	[U4154A	U4154A	U4154A]
Slot 4	[U4154A	U4154A, U4301A, or U4998A	U4154A]
Slot 3	[U4154A	U4154A, U4301A, or U4998A	U4154A, U4301A, or U4998A
Slot 2	[U4154A	Empty	U4154A, U4301A, or U4998A
Slot 1	U4154A, U4301A, U4998A, or controller	Empty or controller	Empty or controller

- Allowable configurations in M9505A 5-slot chassis.
- Brackets indicate combined U4154As.
- Note: Controller, if used, must be installed in slot 1. Otherwise slot assignments are arbitrary.

Related products	
Model	**Description**
U4301A	PCIe Analyzer
U4998A	HDMI Protocol analyzer/generator
FS2430 series DDR3 Detective	FuturePlus DDR3 Detective™ For Use With Keysight Logic Analyzers and Oscilloscopes
FS2501B	FuturePlus DDR4 DIMM Interposer
FS2502B	FuturePlus DDR4 SODIMM Interposer

Ordering Information

Model	Description
U4154A Option 02G	Logic Analyzer, 136-channel, 12.5 GHz timing zoom, 2.5 GHz state, 2 Mb depth
Option 002	2 M sample memory depth (standard)
Option 004	4 M sample memory depth
Option 008	8 M sample memory depth
Option 016	16 M sample memory depth
Option 032	32 M sample memory depth
Option 064	64 M sample memory depth
Option 128;	128 M sample memory depth
Option 200	200 M sample memory depth
M9502A	AXIe 2-slot chassis
M9505A	AXIe 5-slot chassis
U4201Ah	Logic Analyzer Cable For Use With Individual Probes (4 required)
E5861A	Multiframe cable
M9536A	AXIe Embedded PC Controller
M9536A-M16	Memory upgrade from 8 GB RAM to 16 GB RAM
M9536A-W73	Windows 7 operating system (32 bit)
M9536A-W76	Windows 7 operating system (64 bit)
Probes	
W3631A	W3631A DDR3 x16 BGA Command and Data Probe for Logic Analyzer and Scope
W3633A	W3633A DDR3 x4/x8 BGA Command and Data Probe for Logic Analyzer and Scope
E5847A	46-Channel ZIF Probe - Single-ended, for DDR3 x4/x8 DRAM BGA probe connection to 90-pin logic analyzer cable
E5845A	46-Channel ZIF Probe - Single-ended, for DDR3 x16 DRAM BGA probe connection to 90-pin logic analyzer cable
E5406A	Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin cable (34 channels)
E5405A	Pro Series Soft Touch Connectorless Probe - Differential, for 90-pin cable (17 channels)
E5402A	Low Profile, Pro Series Soft Touch Connectorless Probe - Single-ended, for 90-pin cable
E5390A	Soft Touch Connectorless, with 90-pin cable connectors Probe - Single-ended
E5398A	Half-Size Soft Touch Connectorless Probe with 90-pin cable connectors
E5387A	Soft Touch Connectorless, with 90-pin cable connectors Probe - Differential
E5381A	Differential Flying Leads, 17 channels
E5382A	Single-ended Flying Leads, 17 channels
E5378A	Samtec with 90-pin cable connectors Probe - Single-ended
E5379A	Samtec with 90-pin cable connectors Probe - Differential
E5380A	Mictor with 90-pin cable connectors Probe - Single-ended
Nexus Technology NT-DDR3DIHS	DDR3 2133 DIMM interposer
Nexus Technology NT-DDR3SOIHS	DDR3 1600 SODIMM interposer
Nexus Technology NT-DDR3MDI	DDR3-1600 miniDIMM slot interposer
FuturePlus FS2352	DDR3 1867 DIMM interposer
FuturePlus FS2352B	DDR3 2133 DIMM interposer
FuturePlus FS2354	DDR3 1600 SODIMM interposer
FuturePlus FS2501B	DDR4 2133 DIMM interposer
FuturePlus FS2502B	DDR4 1867 SODIMM interposer

Ordering Information (continued)

Model	Description
DDR analysis software	
B4621B	Bus Decoder for DDR2, DDR3, or DDR4 Validation
B4622B	DDR2/3/4 or LPDDR/2/3 Protocol Compliance Toolset
B4623B	Bus Decoder for LPDDR, LPDDR2, or LPDDR3 Validation
Other software	
B4602A	Signal Extractor Tool
B4655A	FPGA dynamic probe for Xilinx
B4656A	FPGA dynamic probe for Altera
B4601C	Serial-to-parallel analysis package
B4606A	Advanced customization environment – development and runtime package
B4607A	Advanced customization environment – runtime package
B4608A	ASCII remote programming interface
ASCII remote programming interface	Data import package
B4630A	MATLAB® connectivity and analysis package
Upgrades	
U4154U option 004	Upgrade memory to 4 M
U4154U option 008	Upgrade memory to 8 M
U4154U option 016	Upgrade memory to 16 M
U4154U option 032	Upgrade memory to 32 M
U4154U option 064	Upgrade memory to 64 M
U4154U option 128	Upgrade memory to 128 M
U4154U option 200	Upgrade memory to 200 M

Calibration

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Select Keysight calibration plan	
R1282A R-50C-011-3	3-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 3 years; 15% cheaper than buying stand-alone calibrations.
R1282A R-50C-011-5	5-year calibration assurance plan (return to Keysight): Priority calibration service covering all calibration costs for 5 years; 20% cheaper than buying stand-alone calibrations.
R1282A R-50C-021-3	ANSI Z540-1-1994 calibration – 3 years
R1282A R-50C-021-5	ANSI Z540-1-1994 calibration – 5 years

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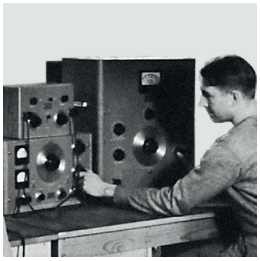

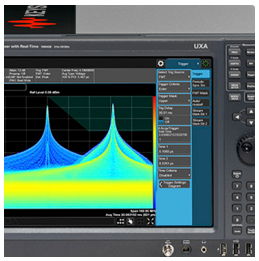

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